Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-12. (Canceled)

13. (New) A computer-implemented method for physical synthesis of integrated circuits, the method comprising:

receiving information indicative of an integrated circuit;

tracing signal flow in the integrated circuit to determine a set of critical signal paths;

placing and routing one or more circuit cells in a physical layout associated with the integrated circuit based on a priority associated with a critical signal path in the set of critical signal paths.

14. (New) The method of claim 13 wherein placing and routing the one or more circuit cells in the physical layout associated with the integrated circuit based on path priorities associated with paths in the set of critical signal paths comprises placing and routing one or more elements of an RF circuit.

15. (New) A computer-implemented method for physical synthesis of integrated circuits, the method comprising:

receiving information indicative of an integrated circuit;

generating a plurality of circuit layout constraints using an open circuit time constant technique on each node in a plurality of critical nodes associated with the integrated circuit;

tracing signal flow within the integrated circuit to determine a set of critical signal paths;

partitioning the physical layout associated with the integrated circuit based on functionality and criticality; and

placing and routing one or more circuit cells automatically in the physical layout associated with the integrated circuit based on a priority associated with a critical signal path in the set of critical signal paths.

16. (New) The method of claim 15 further comprising:

calculating equivalent resistive impedance at each node of in the plurality of critical nodes in response to a DC operating point simulation.

17. (New) The method of claim 15 further comprising:

calculating equivalent resistive impedance at each node in the plurality of critical nodes in response to a transient simulation.

18. (New) The method of claim 15 wherein generating the plurality of circuit layout constraints using the open circuit time constant technique on each node in the plurality of critical nodes associated with the integrated circuit comprises assessing a time constant of each node in the plurality of critical nodes.

19. (New) The method of claim 18 further comprising:

estimating a circuit bandwidth based on the time constant at each node in the plurality of critical nodes;

comparing the estimated circuit bandwidth with a series of design specifications associated with the integrated circuit.

20. (New) The method of claim 15 wherein generating the plurality of circuit layout constraints using the open circuit time constant technique on each node in the plurality of critical nodes associated with the integrated circuit comprises determining an optimal range for parasitic loading values.

21. (New) The method of claim 15 wherein placing and routing the one or more circuit cells automatically in the physical layout associated with the integrated circuit based on the priority associated with the critical signal path in the set of critical signal paths comprises placing and routing the one or more cells in response to one or more what-if scenarios associated with placement options.

22. (New) The method of claim 15 wherein generating the plurality of layout constraints using the open circuit time constant technique on each node in the plurality of critical nodes associated with the integrated circuit comprises calculating a tolerable excessive parasitic loading at each node in the plurality of nodes for circuit physical synthesis at an initial topology exploration stage.

23. A computer readable medium configured to store a software program executable by a processor of a computer system to become operational with the processor for physical synthesis of integrated circuits, the computer readable medium comprising:

program code for receiving information indicative of an integrated circuit;

program code for generating a plurality of circuit layout constraints using an open circuit time constant technique on each node in a plurality of critical nodes associated with the integrated circuit;

program code for tracing signal flow within the integrated circuit to determine a set of critical signal paths;

program code for partitioning the physical layout associated with the integrated circuit based on functionality and criticality; and

program code for placing and routing one or more circuit cells automatically in the physical layout associated with the integrated circuit based on a priority associated with a critical signal path in the set of critical signal paths.